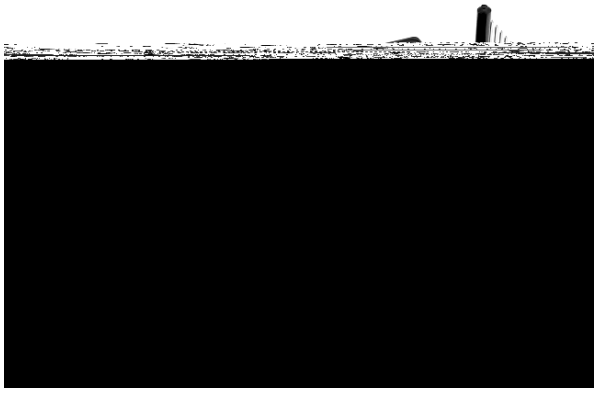
PM450DV1A120

FLAT-BASE TYPE
INSULATED PACKAGE

PM450DV1A120



FEATURE

a) Adopting new 5th generation Full-Gate CSTBT™ chip

b) The over-temperature protection which detects the chip surface temperature of CSTBT™ is adopted.

c) Error output signal is possible from all each protection upper and lower arm of IPM.

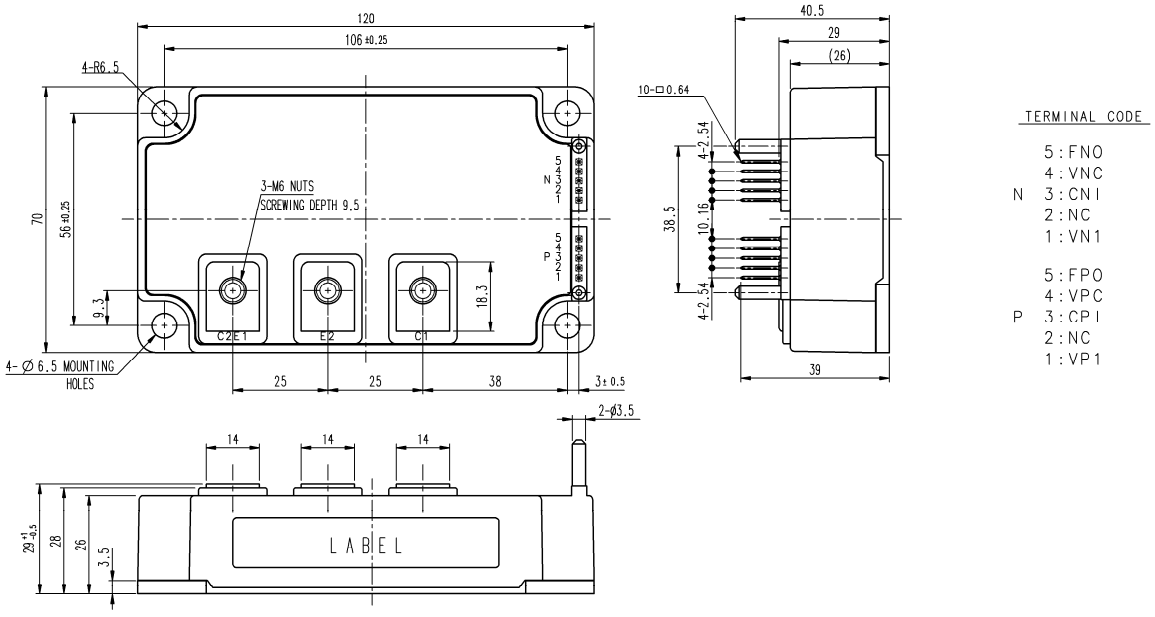
d) Compatible V-series package.

- Monolithic gate drive & protection logic
- Detection, protection & status indication circuits for, short-circuit, over-temperature & under-voltage.

APPLICATION

General purpose inverter, servo drives and other motor controls

PACKAGE OUTLINES **Dimensions in mm**



MITSUBISHI ELECTRIC

INTERNAL FUNCTIONS BLOCK DIAGRAM

TOTAL SYSTEM

Symbol	Parameter	Conditions	Ratings	Unit
$V_{CC(PROT)}$	Supply Voltage Protected by SC	V_D =13.5V ~ 16.5V Inverter Part, T_j =+125°C Start	800	V
$V_{CC(surge)}$	Supply Voltage (Surge)	Applied between : C1-E2, Surge value	1000	V

CONTROL PART

Symbol	Parameter	Conditions		Limits			Unit
				Min.	Typ.	Max.	
I_D	Circuit Current	V_D=15V, V_{CIN}=15V	V_{P1}-V_{PC}	-	2	4	mA
			V_{N1}-V_{NC}	-	2	4	
$V_{th(ON)}$	Input ON Threshold Voltage	Applied between : C_{PI}-V_{PC}, C_{NI}-V_{NC}		1.2	1.5	1.8	V
$V_{th(OFF)}$	Input OFF Threshold Voltage			1.7	2.0	2.3	

PRECAUTIONS FOR TESTING

1. Before applying any control supply voltage (V_D), the input terminals should be pulled up by resistors, etc. to their corresponding supply voltage and each input signal should be kept off state.
   After this, the specified ON and OFF level setting for each input signal should be done.
2. When performing “SC” tests, the turn-off surge voltage spike at the corresponding protection operation should not be allowed to rise above V_{CES} rating of the device.
   (These test should not be done by using a curve tracer or its equivalent.)

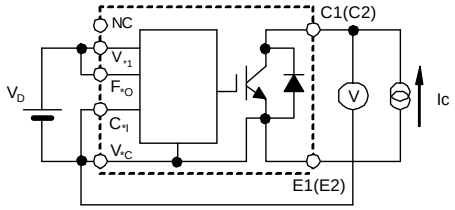


Fig. 1 V_{CEsat} Test

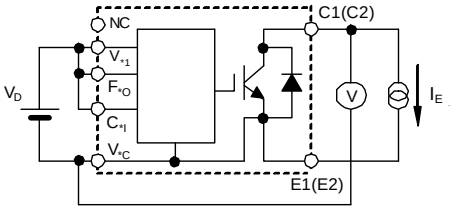


Fig. 2 V_{EC} Test

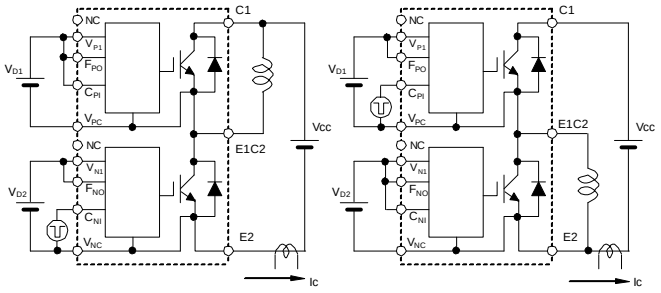


Fig. 3 Switching time and SC test circuit

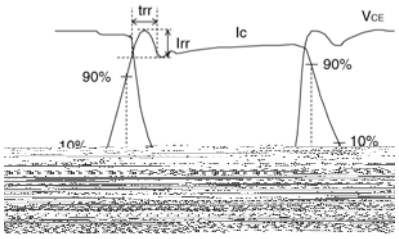


Fig. 4 Switching time test waveform

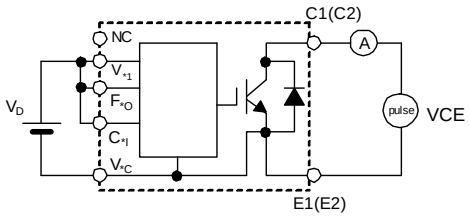


Fig. 5 I_{CES} Test

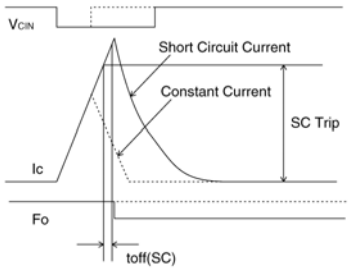
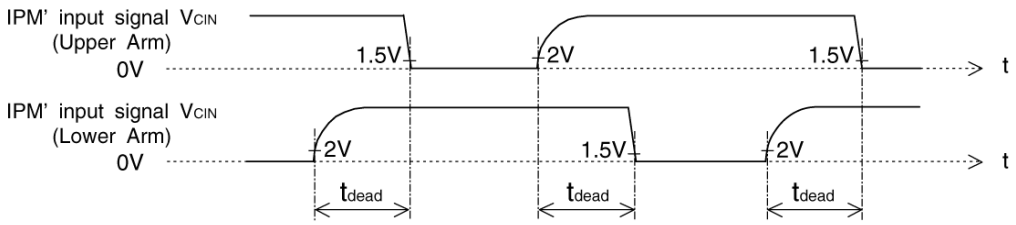


Fig. 6 SC test waveform



1.5V: Input on threshold voltage Vth(on) typical value, 2V: Input off threshold voltage Vth(off) typical value

Fig. 7 Dead time measurement point example

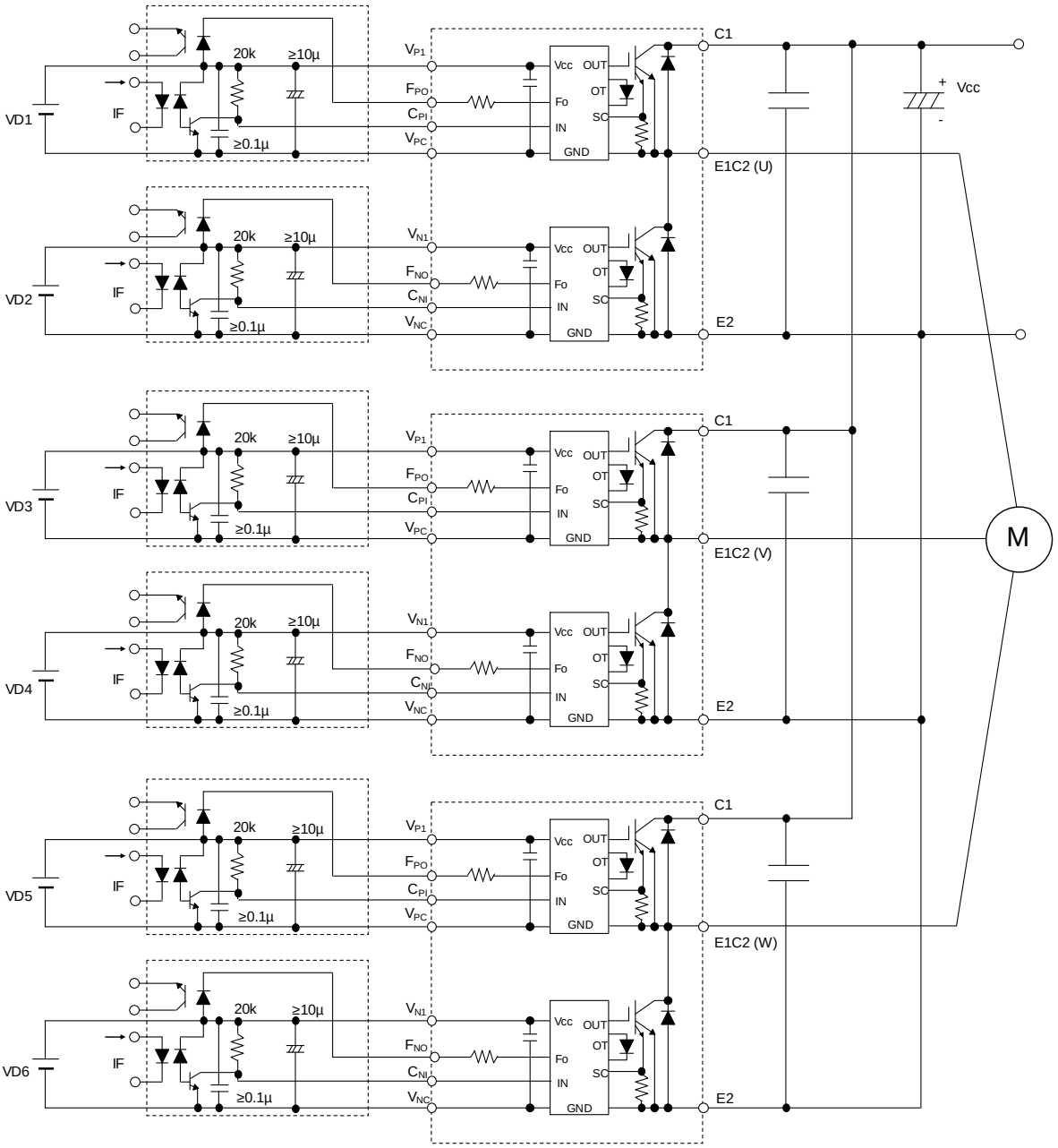
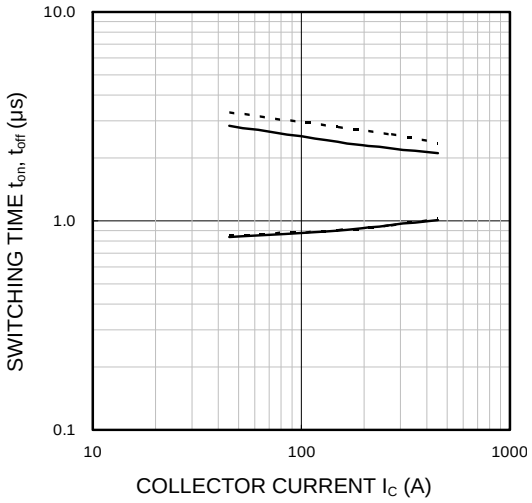


Fig. 8 Application Example Circuit

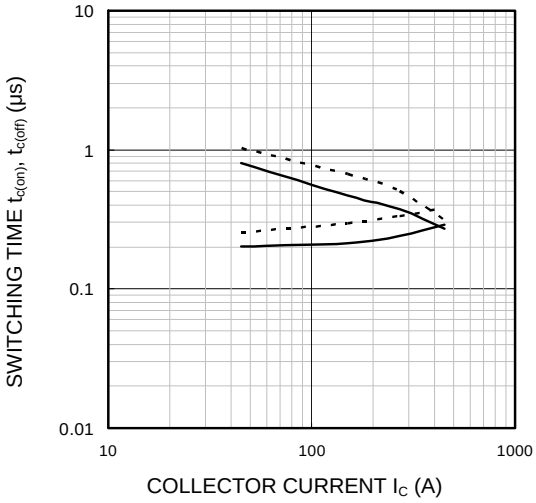
NOTES FOR STABLE AND SAFE OPERATION ;

- Design the PCB pattern to minimize wiring length between opto-coupler and IPM's input terminal, and also to minimize the stray capacity between the input and output wirings of opto-coupler.
- Connect low impedance capacitor between the Vcc and GND terminal of each fast switching opto-coupler.
- Fast switching opto-couplers: t_{PLH}, t_{PHL} ≤ 0.8μs, Use High CMR type.
- Slow switching opto-coupler: CTR > 100%
- Use 6 isolated control power supplies (V_D). Also, care should be taken to minimize the instantaneous voltage charge of the power supply.
- Make inductance of DC bus line as small as possible, and minimize surge voltage using snubber capacitor between C1 and E2 terminal.

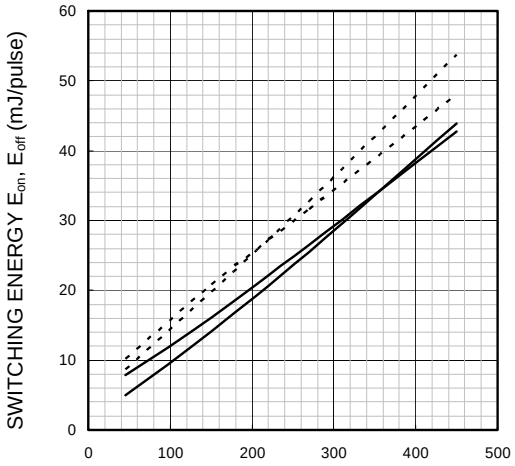
SWITCHING TIME (t_{on}, t_{off}) CHARACTERISTICS (TYPICAL)



SWITCHING TIME ($t_{c(on)}$, $t_{c(off)}$) CHARACTERISTICS (TYPICAL)



SWITCHING ENERGY CHARACTERISTICS (TYPICAL)



FREE WHEELING DIODE REVERSE RECOVERY CHARACTERISTICS (TYPICAL)

FREE WHEELING DIODE
REVERSE RECOVERY ENERGY CHARACTERISTICS
(TYPICAL)

REVESE RECOVERY ENERGY E_{rr} (mJ/pulse)

I_D VS. f_c CHARACTERISTICS
(TYPICAL)

TRANSIENT THERMAL IMPEDANCE CHARACTERISTICS

NORMALIZED TRANSIENT THERMAL IMPEDANCE $Z_{th(j-c)}$